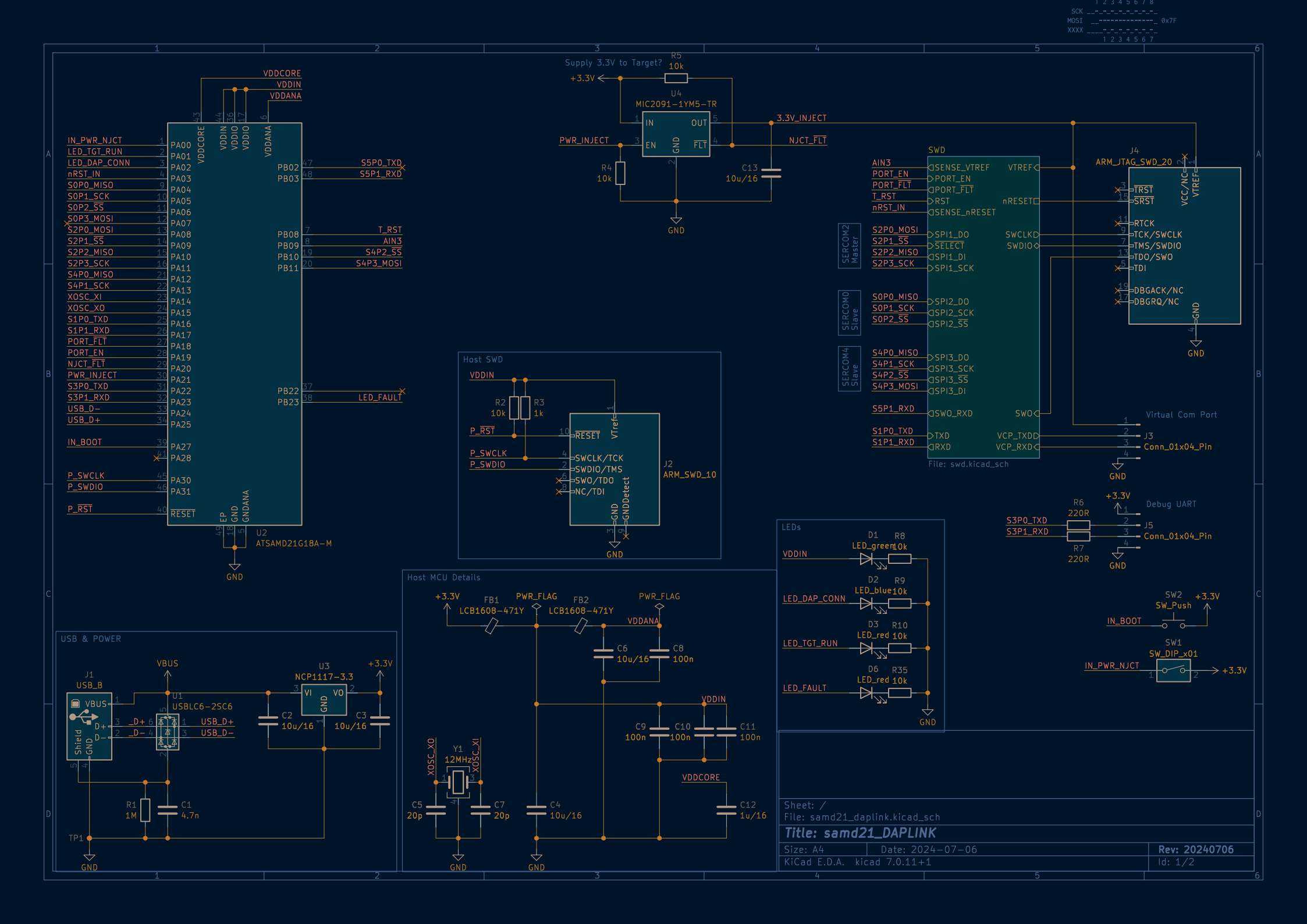

VDDCORE
VDDIN
VDDANA
U2
ATSAMD21G18A-M
IN_PWR_NJCT
LED_TGT_RUN
LED_DAP_CONN
nRST_IN
S0P0_MISO
S0P1_SCK
S0P2_SS
S0P3_MOSI
S2P0_MOSI
S2P1_SS
S2P2_MISO
S2P3_SCK
S4P0_MISO
S4P1_SCK
XOSC_XI
XOSC_XO
S1P0_TXD
S1P1_RXD
PORT_FLT
PORT_EN
NJCT_FLT
PWR_INJECT
S3P0_TXD
S3P1_RXD
USB_D-
USB_D+
IN_BOOT
P_SWCLK
P_SWDIO
P_RST
S5P0_TXD
S5P1_RXD
T_RST
AIN3
S4P2_SS
S4P3_MOSI
LED_FAULT
GND
Supply 3.3V to Target?
R5
10k
+3.3V
U4
MIC2091-1YM5-TR
IN
OUT
EN
GND
FLT
3.3V_INJECT
NJCT_FLT
R4
10k
C13
10u/16
SWD
AIN3
PORT_EN
PORT_FLT
T_RST
nRST_IN
S2P0_MOSI
S2P1_SS
S2P2_MISO
S2P3_SCK
S0P0_MISO
S0P1_SCK
S0P2_SS
S4P0_MISO
S4P1_SCK
S4P2_SS
S4P3_MOSI
S5P1_RXD
S1P0_TXD
S1P1_RXD
SENSE_VTREF
SENSE_nRESET
SPI1_DO
SPI1_SELECT
SPI1_DI
SPI1_SCK
SPI2_DO
SPI2_SCK
SPI2_SS
SPI3_DO
SPI3_SCK
SPI3_SS
SPI3_DI
SWO_RXD
TXD
RXD
VTREF
nRESET
SWCLK
SWDIO
SWO
VCP_TXD
VCP_RXD
SERCOM2 Master
SERCOM0 Slave
SERCOM4 Slave
File: swd.kicad_sch
J4
ARM_JTAG_SWD_20
TRST
SRST
RTCK
TCK/SWCLK
TMS/SWDIO
TDO/SWO
TDI
DBGACK/NC
DBGRQ/NC
VCC/NC
VTREF
Virtual Com Port
J3
Conn_01x04_Pin
Host SWD
R2
10k
R3
1k
P_RST
P_SWCLK
P_SWDIO
RESET
SWCLK/TCK
SWDIO/TMS
SWO/TDO
NC/TDI
GNDDetect
VTref
J2
ARM_SWD_10
R6
220R
R7
220R
Debug UART
J5
Conn_01x04_Pin
LEDs
D1
LED_green
R8
10k
D2
LED_blue
R9
10k
D3
LED_red
R10
10k
D6
LED_red
R35
10k
SW2
SW_Push
SW1
SW_DIP_x01
USB & POWER
J1
USB_B
VBUS
Shield
GND
D+
D-
U1
USBLC6-2SC6
U3
NCP1117-3.3
VI
VO
C2
10u/16
C3
10u/16
R1
1M
C1
4.7n
TP1
Host MCU Details
FB1
LCB1608-471Y
FB2
LCB1608-471Y
PWR_FLAG
C6
10u/16
C8
100n
C9
100n
C10
100n
C11
100n
C12
1u/16
C4
10u/16
C5
20p
C7
20p
Y1
12MHz
XOSC_XO
XOSC_XI
Sheet: /
File: samd21_daplink.kicad_sch
Title: samd21_DAPLINK
Size: A4
Date: 2024-07-06
Rev: 20240706
KiCad E.D.A. kicad 7.0.11+1
Id: 1/2

PORT_EN = 0, should put the
JTAG/SWD pins into Hi-Z
state... that is:
TCK TMS TDI TDO nTRST nRESET

Level Shifting
- Debugger: 3.3V
- Target: 1.8 to 5.5V

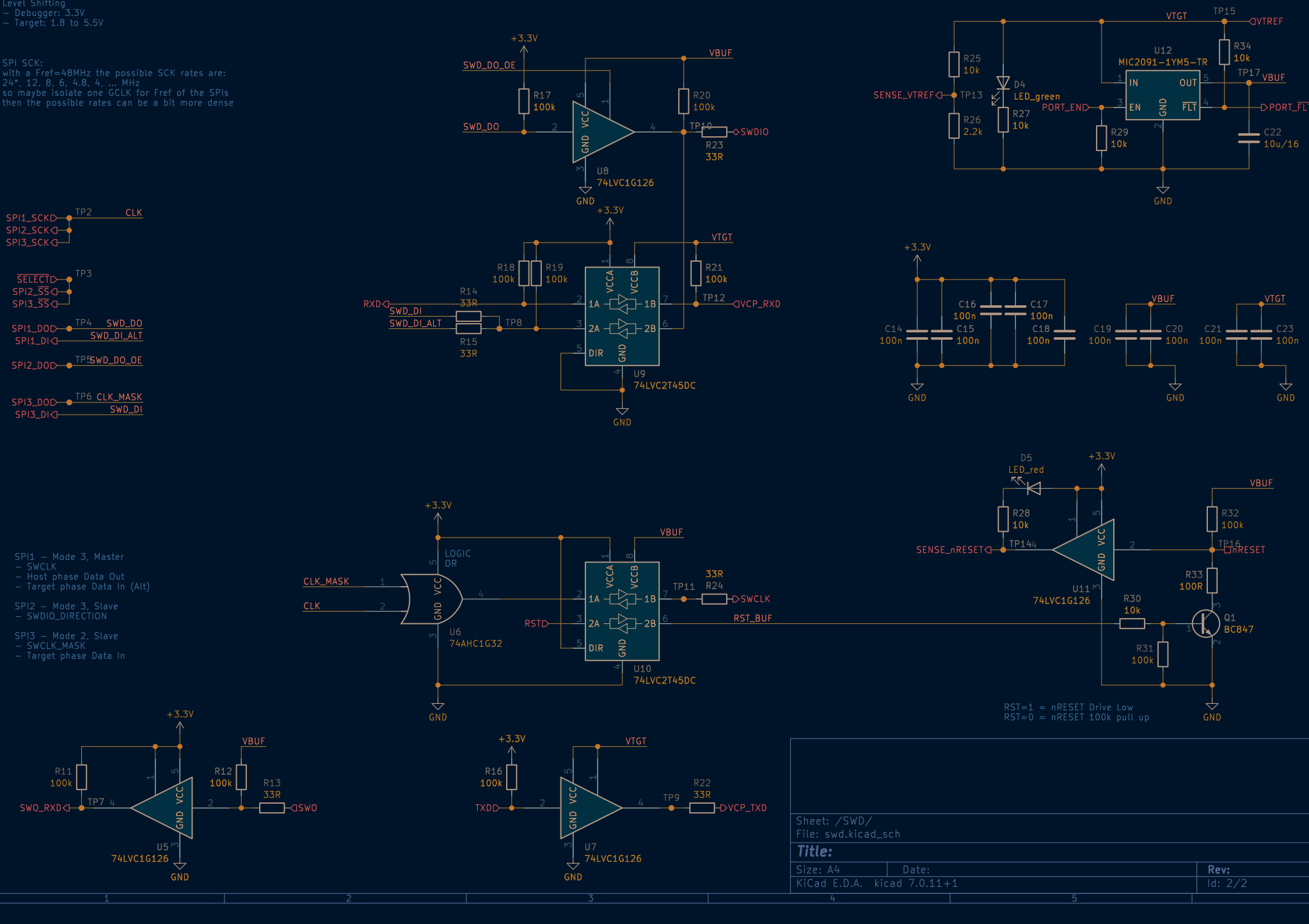
SPI SCK:
with a Fref=48MHz the possible SCK rates are:
24*, 12, 8, 6, 4.8, 4, ... MHz
so maybe isolate one GCLK for Fref of the SPIs
then the possible rates can be a bit more dense

SPI1 – Mode 3, Master
- SWCLK
- Host phase Data Out
- Target phase Data In (Alt)

SPI2 – Mode 3, Slave
- SWDIO_DIRECTION

SPI3 – Mode 2, Slave
- SWCLK_MASK
- Target phase Data In

RST=1 = nRESET Drive Low
RST=0 = nRESET 100k pull up



Sheet: /SWD/
File: swd.kicad_sch

Title:

Size: A4 | Date: | **Rev:**
KiCad E.D.A. kicad 7.0.11+1 | Id: 2/2